CLAIMS:

What is claimed is:

1. A method in a data processing system for isolating a defect in a memory system to a particular memory system component, said method comprising the steps of:

said memory system including a plurality of components, said plurality of components including a physical memory module coupled to a memory card, said memory card, and a memory controller for controlling said memory card; and

testing each one of said plurality of components separately to identify a defective one of said plurality of components.

2. The method according to claim 1, further comprising the steps of:

testing said physical memory module;

in response to said physical memory module passing said test, testing said memory card; and

in response to said memory card passing said test, testing said memory controller.

3. The method according to claim 2, further comprising the steps of:

said memory card including a buffer; and

wherein said step of testing said memory card includes:

treating said buffer as a virtual memory module; and

testing said memory card utilizing said virtual memory module.

4. The method according to claim 2, further comprising the steps of:

said memory card including a buffer; and

wherein said step of testing said physical memory module includes:

treating said buffer as a virtual memory controller; and

testing said physical memory module utilizing said virtual memory controller.

5. The method according to claim 2, further comprising the steps of:

said memory card including a buffer; and

wherein said step of testing said memory card includes:

treating said buffer as a virtual memory module; and

testing said memory card utilizing said buffer by writing a data pattern to said memory card to be stored in said virtual memory module;

said step of testing said memory card including:

storing said data pattern in said virtual memory module;

reading a data pattern from said virtual memory;

comparing said data pattern written to said virtual memory module to said data pattern read from said virtual memory module;

determining that said memory card passed said test in response to said data pattern written to said virtual memory module being the same as said data pattern read from said virtual memory module; and

determining that said memory card failed said test in response to said data pattern written to said virtual

memory module being different from said data pattern read from said virtual memory module.

6. The method according to claim 3, further comprising the steps of:

said memory card including a plurality of buffers; and

assigning a unique identifier to each one of said plurality of buffers for addressing said plurality of buffers.

7. The method according to claim 3, further comprising the steps of:

coupling said buffer to a service processor; and

testing, utilizing said service processor, said memory card.

8. The method according to claim 7, further comprising the steps of:

coupling said buffer to said service processor utilizing a JTAG bus.

9. The method according to claim 2, further comprising the steps of:

storing a data pattern in said memory controller;

reading a data pattern from said memory controller;

comparing said data pattern written to said memory controller to said data pattern read from said memory controller;

determining that said memory controller passed said test in response to said data pattern written to said

memory controller being the same as said data pattern read from said memory controller; and

determining that said memory controller failed said test in response to said data pattern written to said memory controller being different from said data pattern read from said memory controller.

10. The method according to claim 9, further comprising the steps of:

coupling said memory controller to a service processor.

11. The method according to claim 9, further comprising the steps of:

coupling said memory controller to a service processor utilizing a JTAG bus.

12. The method according to claim 2, further comprising the steps of:

said memory card including a tristate device; and

wherein said step of testing said memory card includes:

treating said tristate device as a virtual memory module; and

testing said memory card utilizing said virtual memory module.

13. The method according to claim 12, further comprising the steps of:

said memory card including a tristate device; and

wherein said step of testing said memory card includes:

treating said tristate device as a virtual memory module; and

testing said memory card utilizing said virtual memory module by writing a data pattern to said memory card;

said step of testing said memory card including:

storing said data pattern in said tristate device;

reading a data pattern from said tristate device;

comparing said data pattern written to said tristate device to said data pattern read from said tristate device;

determining that said memory card passed said test in response to said data pattern written to said tristate device being the same as said data pattern read from said tristate device; and

determining that said memory card failed said test in response to said data pattern written to said tristate device being different from said data pattern read from said tristate device.

14. A data processing system for isolating a defect in a memory system to a particular memory system component, said system comprising:

said memory system including a plurality of components, said plurality of components including a physical memory module coupled to a memory card, said memory card, and a memory controller for controlling said memory card; and

logic that tests each one of said plurality of components separately to identify a defective one of said plurality of components.

15. The system according to claim 14, further comprising:

logic that tests said physical memory module;

in response to said physical memory module passing said test, logic that tests said memory card; and

in response to said memory card passing said test, logic that tests said memory controller.

16. The system according to claim 15, further comprising:

said memory card including a buffer; and

wherein said logic that tests said memory card includes:

said buffer acting as a virtual memory module; and

logic that tests said memory card utilizing said virtual memory module.

17. The system according to claim 15, further comprising:

said memory card including a buffer; and

wherein said logic that tests said memory card includes:

said buffer acting as a virtual memory module; and

logic that tests said memory card utilizing said buffer by writing a data pattern to said memory card to be stored in said virtual memory module;

said logic that tests said memory card including:

storing means for storing said data pattern in said virtual memory module;

reading means for reading a data pattern from said virtual memory;

comparing means for comparing said data pattern written to said virtual memory module to said data pattern read from said virtual memory module;

determining means for determining that said memory card passed said test in response to said data pattern written to said virtual memory module being the same as said data pattern read from said virtual memory module; and

determining means for determining that said memory card failed said test in response to said data pattern written to said virtual memory module being different from said data pattern read from said virtual memory module.

18. The system according to claim 16, further comprising:

said memory card including a plurality of buffers; and

assigning means for assigning a unique identifier to each one of said plurality of buffers for addressing said plurality of buffers.

19. The system according to claim 16, further comprising:

said buffer being coupled to a service processor; and

said service processor for testing said memory card.

20. The system according to claim 19, further comprising:

said buffer being coupled to said service processor utilizing a JTAG bus.

21. The system according to claim 15, further comprising:

storing means for storing a data pattern in said memory controller;

reading means for reading a data pattern from said memory controller;

comparing means for comparing said data pattern written to said memory controller to said data pattern read from said memory controller;

determining means for determining that said memory controller passed said test in response to said data pattern written to said memory controller being the same as said data pattern read from said memory controller; and

determining means for determining that said memory controller failed said test in response to said data pattern written to said memory controller being different from said data pattern read from said memory controller.

22. The system according to claim 21, further comprising:

said memory controller being coupled to a service processor utilizing a JTAG bus.

23. The system according to claim 15, further comprising:

said memory card including a tristate device; and

wherein said logic that tests said memory card includes:

said tristate device acting as a virtual memory module; and

logic that tests said memory card utilizing said virtual memory module.

24. The system according to claim 15, further comprising:

said memory card including a buffer; and

wherein said logic that tests said physical memory module includes:

said buffer acting as a virtual memory controller; and

logic that tests said physical memory module utilizing said buffer acting as said virtual memory controller.

25. A computer program product in a data processing system for isolating a defect in a memory system to a particular memory system component, said product comprising:

said memory system including a plurality of components, said plurality of components including a physical memory module coupled to a memory card, said memory card, and a memory controller for controlling said memory card; and

instruction means for testing each one of said plurality of components separately to identify a defective one of said plurality of components.

26. The product according to claim 25, further comprising:

instruction means for testing said physical memory module;

in response to said physical memory module passing said test, instruction means for testing said memory card; and

in response to said memory card passing said test, instruction means for testing said memory controller.

27. The product according to claim 26, further comprising:

said memory card including a buffer; and

wherein said instruction means for testing said memory card includes:

instruction means for treating said buffer as a virtual memory module; and

instruction means for testing said memory card utilizing said virtual memory module.